General information	**Title and code of subject, number of credits**	ETR 463 Digital Microelectronics 6 ECTS	
	Department	Physics & Electronics	
	Program	Bachelor	
	Academic semester	Fall, 2022	
	Lecturer	M.Sc Babak Emdadi	
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	Lecture room/Schedule	11 Mehseti Street, (Neftchilar campus)	
	Consultations		
Course language	English		
Type of the subject	Major		
Textbooks and additional materials	***Textbooks*:** 1. Rabaey, Chandrakasan & Nikolil, "Digital Integrated Circuits," Prentice Hall, 2nd edition, 2003. 2. Neil H. E. Weste & David Harris, "CMOS VLSI design: a circuits and systems perspective," Addison Wesley, 3rd edition, 2004.		
Teaching methods	**Lecture**		x
	Group discussion		x
	Experiential exercise		-
	Quiz, Classroom Exams		x
Assessment	**Components**	**Date/ Deadline**	**Percent (%)**
	Active participation	At each lesson	10
	Quizzes	During the semester	10
	Attendance		10
	Midterm exam		30
	Final exam		40
	Final		**100**
Course outline	This course examines the design and technologies underlying modern digital microelectronic systems. The list of topics include: Introduction to fabrication processes; Design rules (revisited); Transistor models.		
Course objectives	This course aims to design and technologies underlying modern digital microelectronic systems.		
Learning outcomes (LO))	On successful completion of this course students will be able to: 1. Design digital logic gates and standard cells at transistor schematic and corresponding layouts level in CMOS technology using CMOS logic gates, pseudo-nMOS, footed and footless domino logic families. 2. Explain and evaluate the effect of the parasitic and loading on CMOS circuit operation and performance in terms of size, area and noise margin and ways to minimise delay. 3. Model the effect of interconnect upon a design and to apply strategies to mitigate problems arising from interconnect loading. 4. Explain the function of CMOS memory circuits and design basic CMOS ROM and PLA circuits. 5. Explain factors that influence circuit reliability and be able to apply reasonable design margins. 6. Demonstrate team work to design a system module		

Rules (Educational policy and behavior)	▪ **Preparation for class** The structure of this course makes your individual study and preparation outside the class extremely important. The lecture material will focus on the major points introduced in the text. Reading the assigned chapters and having some familiaritywith them before class will greatly assist your understanding of the lecture. Afterthe lecture, you should study your notes and work relevant problems and cases from the end of the chapter and sample exam questions. • **Withdrawal (pass/fail)** This course strictly follows grading policy of the School of Humanities, Education and Social sciences. Thus, a student is normally expected to achieve a mark of at least 60% to pass. In case of failure, he/she will be required to repeat the course the following term or year. ▪ **Cheating/plagiarism** Cheating or other plagiarism during the Quizzes, Mid-term and Final Examinations will lead to paper cancellation. In this case, the student will automatically get zero (0), without any considerations. ▪ **Professional behavior guidelines** The students shall behave in the way to create favorable academic and professional environment during the class hours. Unauthorized discussions and unethical behavior are strictly prohibited. **Attendance** Students who attend the whole classes will get 5 marks. for three absence student loses 1 mark. • **Quizzes** There will be a quizzes per two weeks. The quizzes will be announced in the classroom two weeks before and will relate to homework. • **Activity** Students who will be active during discussion of past lessons will be awarded with one activity mark.

This program reflects the comprehensive information about the subject and information about any changes will be provided in advance.

Week	Dates (planned)	Subject topics	Textbook/ Assignments
1		Introduction to the course and presentation of practical structure	[2] p. 2-16
2		Introduction to fabrication processes, design rules (revisted). Transistor models (revisited from third year electronics) and layout issues and ASIC design flow	[1] p. 4-20 [1] p.30-52 [1] p. 24-28 [1] p. 67-81
3		VLSI design methodology and leaf cell design	[2] p. 31-57 [2] p. 76-85
4		Performance estimation of CMOS complex gates and interconnected modules using logical effort	[2] p. 113-146 [2] p. 153-155
5		Static and dynamic CMOS logic families and adders design	[1] p. 216-240 [3] p. 124-148

		Quiz 1(Lec1-Lec4)	[1] p. 242-251
6		Memory structures and operation	[2] p. 173-198 [2] p. 201-208 [2] p. 201-208
7		Low power design and system level consideration ***Quiz 2(Lec5-Lec6)***	[2] p. 271-300 [2] p. 310-314
8		***Mid-term exam***	
9		Demonstrating the design of CMOS gates and transistor sizing	[2] p. 384-422 [2] p. 425-427
10		CMOS circuits layout and delay estimation	[2] p. 565-588 [2] p. 596-600
11		CMOS circuits delay estimation using logical effort ***Quiz 3 (Lec9-Lec10)***	[2] p. 602-635 [2] p. 667-693 [2] p. 636-638 [2] p. 694-698
12		Delay path estimation using logical effort	[2] p. 764-788 [2] p. 801-805
13		PLA and memory Design	[2] p. 807-825 [2] p. 845-850
14		***Recap of all covered material*** ***Quiz 4 (Lec11-Lec13)***	
15		Solving problems and ambiguities of students about the course Solving extra examples	
		Final Exam