Identification	Subject	ETP 220 Digital electronics 6 ECTS of	radita		
Identification	Subject (code, title,	ETR 320 Digital electronics-6 ECTS cr	realts		
	credits)				
	Department	Physics and Electronics			
	Program	Undergraduate			
	(undergraduate,				
	graduate)				
	Term	Fall 2022			
	Instructor	Ahmad Asimov ph.D			
	E-mail:	fizikasimov@gmail.com			
	Phone: Classroom/hours	+994124211093 (daxili255)			
	Office hours	302N Monday /Wednesday Tuesday: 15:00-16:00/ Thursday: 15:0	00-16.00		
Prerequisites	Office nours	Tuesday. 15.00-10.00/ Thursday. 15.0	00-10.00		
Language	English				
Compulsory	Compulsory				
Required textbooks	John F. Wakerly, Digital Design: Principles and Practices, 5/e, Pearson, 2018				
and course materials	William Kleitz, Digital Electronics, Prentice Hall International Inc.				
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Course outline	The purpose of the course is to teach principles of digital electronics. Among the topics				
	discussed are number systems, codes, logic gates, Boolean statements, combinational				
	logic, flip-flops, counters, shift registers, memory and storage, and integrated circuit				
	technologies. Students should be able to analyze, and design combinational and sequential circuits.				
Course objectives	* -				
Course objectives					
	understand digital electronics circuits. Verifying and analyzing the practical digital circuits. Understanding the minimization of logic expression and designing combinational and sequential digital circuits				
Learning outcomes	On successful compl	etion of this course students will be able	to:		
	1. Perform basic	arithmetic calculations in binary, decimal	and hexadecimal;		
	 Analyze and synthesize combinational logic circuits; Analyze the basic operation of memory cell and its limitations in circuit designing. Program a microcontroller to control a simple physical system and to perform simple digital transformations to an analog signal; Select, justify and use appropriate input and output devices and controllers for 				
	simple digital systems;				
Teaching methods	Lecture				
	Group discussion				
	Experiential exercise				
Fueluation	Quiz, Classroom Ex Methods		Demonstrage (0/2)		
Evaluation	Midterm Exam	Date/deadlines	Percentage (%) 30		
		At the each lesser			
	Attendance	At the each lesson	5		
	Attendance Quizzes	4 quizzes during the semester	5 20		
	Attendance Quizzes Activity		5 20 5		
	Attendance Quizzes	4 quizzes during the semester	5 20		

Polic	cy					
		eparation outside the class points introduced in the with them before class will e, you should study your e chapter and sample				
		• Withdrawal (pass/fail) This course strictly follows grading policy of the School of Science and Engineering. Thus, a student is normally expected to achieve a mark of at least 60% to pass. In case of failure, he/she will be required to repeat the course the following term or year.				
		• Cheating/plagiarism Cheating or other plagiarism during the Quizzes, Mid-term and Final Examinations will lead to paper cancellation. In this case, the student will automatically get zero (0), without any considerations.				
		• Professional behavior guidelines The students shall behave in the way to create favorable academic and professional environment during the class hours. Unauthorized discussions and unethical behavior are strictly prohibited.				
		 Quizzes There will be a quiz examination per two weeks. The quizzes will be announced in the classroom two weeks before. Quiz is from homework problems. The homework problems will be selected from questions and problems in the end of each chapter. The No. of homework problems will be announced after finishing each chapter. There will be 4 quizzes during the semester . The quizzes will be announced in the classroom two weeks before and will relate to homework. Attendance 				
		 Students who attend the whole classes will get 5 marks. for tw mark. Activity Students who will be active during discussion of past lessor one activity mark. 				
		Tentative Schedule				
Week	Date/Day (tentative)	Topics	Textbook			
1	19.09.22 26.09.22	Introduction: Characteristics of digital systems, Number systems, arithmetical operations with binary numbers Fundamentals of Boolean Algebra Axioms and theorems	Chapter 1			
2	03.10.22 10.10.22	Logic functions, representation, canonical and standard forms. Introduction to Logic Gates: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR and their combinations. Design of adder, subtractors, comparators, code converters, encoders, decoders, multiplexers and de- multiplexers, Function realization using gates & multiplexers.	Chapter 2			
3	17.10.22 24.10.22	Timing diagrams, propagation delays, hazards, minimization of logic functions, essential/sufficient prime implicants, prime implicant chart	Chapter 3			

31.10.22 07.11.22	Incomplete functions, don't cares, general functions, prime implicants using Quine-McCluskey, ICs, half adder, full adder, subtraction, multiplexers	Chapter 4
14.11.22	Midterm	
21.11.22	Sequential Logic Analysis and Design Flip-Flops, Latches and Their Applications. Demultiplexers, decoders, programmable logic devices (PLDs): PLAs, PALs, FPGAs	Chapter 5
28.11.22 05.12.22	Feedback connections. Introduction to Latches and Flip flops – SR, D, JK and T. Design of synchronous sequential circuits – Counters, shift registers. Finite State Machines	Chapter 6
12.12.22 19.12.22	Semiconductor Memories. Introduction and classification of ROM, ROM organization, Static and Dynamic RAM, DRAM Refreshing	Chapter 7
26.12.22	Representative circuits for cells using BJT and FET's, Timing diagrams of memories, Memory expansion using IC's, Flash memory, CCD, Magnetic Memories. Final Exam	Chapter 8
	07.11.22 14.11.22 21.11.22 28.11.22 05.12.22 12.12.22 19.12.22	07.11.22implicants using Quine-McCluskey, ICs, half adder, full adder, subtraction, multiplexers14.11.22Midterm21.11.22Sequential Logic Analysis and Design Flip-Flops, Latches and Their Applications. Demultiplexers, decoders, programmable logic devices (PLDs): PLAs, PALs, FPGAs28.11.22Feedback connections. Introduction to Latches and Flip flops – SR, D, JK and T. Design of synchronous sequential circuits – Counters, shift registers. Finite State Machines12.12.22Semiconductor Memories. Introduction and classification of ROM, ROM organization, Static and Dynamic RAM, DRAM Refreshing26.12.22Representative circuits for cells using BJT and FET's, Timing diagrams of memories, Memory expansion using IC's, Flash memory, CCD, Magnetic Memories.

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